

What Is Claimed Is:

- 1 1. A digital adjustable chip oscillator, comprising:
 - 2 a voltage control oscillator generating an oscillation
 - 3 signal, receiving a control voltage to adjust the
 - 4 frequency of the oscillation signal, and receiving
 - 5 an operating voltage to stabilize the frequency of
 - 6 the oscillation signal;
 - 7 a reference voltage circuit generating a reference
 - 8 voltage;
 - 9 a voltage regulation circuit receiving the reference
 - 10 voltage and generating the operating voltage;
 - 11 a digital tuning circuit receiving a digital code to
 - 12 adjust the control voltage and receiving the
 - 13 operating voltage to stabilize the control
 - 14 voltage;
 - 15 a frequency detector receiving the oscillation signal,
 - 16 a first reference signal with a first frequency,
 - 17 and a second reference signal with a second
 - 18 frequency, wherein when the frequency of the
 - 19 oscillation signal lies between the first
 - 20 frequency and the second frequency, the frequency
 - 21 detector will output a high voltage comparison
 - 22 signal, otherwise the frequency detector will
 - 23 output a low voltage comparison signal;
 - 24 a programmable counter receiving a clock signal to
 - 25 trigger the counting and generating the digital
 - 26 code;
 - 27 a programmable controller receiving the high voltage
 - 28 comparison signal to generate an enable signal
 - 29 directing the frequency detector to hold the high

30 voltage comparison signal and directing the
31 programmable counter to stop counting and hold the
32 digital code; and
33 a programmable memory receiving the enable signal to
34 record the digital code.

1 2. The digital adjustable chip oscillator as claimed
2 in claim 1, wherein the voltage control oscillator is a
3 relaxation oscillator.

1 3. The digital adjustable chip oscillator as claimed
2 in claim 1, wherein the reference voltage circuit is a
3 bandgap reference voltage circuit.

1 4. The digital adjustable chip oscillator as claimed
2 in claim 1, wherein the voltage regulation circuit
3 comprises:
4 an operational transconductance amplifier receiving the
5 reference voltage, receiving a loop voltage, and
6 outputting a bias voltage;
7 a transistor receiving the bias voltage, outputting a
8 current, and outputting the operating voltage; and
9 a loop circuit receiving the current and outputting the
10 loop voltage.

1 5. The digital adjustable chip oscillator as claimed
2 in claim 1, wherein the digital tuning circuit comprises:
3 a plurality of current mirrors receiving a bias voltage
4 to generate a plurality of bias currents
5 corresponding to the bit of the digital code and

6 receiving the operating voltage to stabilize the
7 plurality of bias currents;
8 a transistor receiving the plurality of bias currents
9 to generate the control voltage; and
10 a plurality of switches coupled to the plurality of
11 current mirrors and the transistor and receiving
12 the digital code to select the plurality of
13 current mirrors.

1 6. The digital adjustable chip oscillator as claimed
2 in claim 5, further comprising a prescaler receiving the
3 oscillation signal and generating a period dividing signal
4 according to a period dividing code.

1 7. The digital adjustable chip oscillator as claimed
2 in claim 6, wherein the digital tuning circuit further
3 comprises:
4 an operational transconductance amplifier receiving the
5 reference voltage, receiving a loop voltage, and
6 outputting the bias voltage;
7 a transistor receiving the bias voltage, outputting a
8 reference current, and proportioning the bias
9 current of the plurality of current mirrors to the
10 reference current wherein the bias voltage is
11 coupled to the plurality of current mirrors; and
12 a loop circuit receiving the reference current and
13 outputting the loop voltage.

1 8. The digital adjustable chip oscillator as claimed
2 in claim 1, wherein the digital tuning circuit further
3 comprises:

4 a plurality of charge current mirrors receiving a bias
5 voltage to generate a plurality of bias currents
6 corresponding to the bit of the digital code and
7 receiving the operating voltage to stabilize the
8 plurality of bias currents;
9 a plurality of discharge current mirrors receiving the
10 bias current to generate a plurality of bias
11 currents corresponding to the bit of the digital
12 code;
13 a transistor receiving the plurality of bias currents
14 to generate the control voltage;
15 a plurality of first switches coupled to the plurality
16 of current mirrors and the transistor and
17 receiving the digital code to select the plurality
18 of charge current mirrors; and
19 a plurality of second switches coupled to the plurality
20 of current mirrors and the transistor and
21 receiving the digital code to select the plurality
22 of charge current mirrors.

1 9. The digital adjustable chip oscillator as claimed
2 in claim 1, wherein the programmable memory is a
3 programmable fuse.

1 10. The digital adjustable chip oscillator as claimed
2 in claim 1, wherein the programmable memory is a
3 programmable gate writer.

1 11. The digital adjustable chip oscillator as claimed
2 in claim 1, wherein the frequency detector comprises:

3 a first phase frequency detector receiving the first
4 reference signal, receiving the oscillation
5 signal, and generating a first detection signal;
6 a first low-pass filter receiving the first detection
7 signal and outputting the dc component of the
8 first detection signal;
9 a first comparator receiving the dc component of the
10 first detection signal and generating a first
11 comparison signal wherein when the first reference
12 frequency lies above the oscillation frequency,
13 the first comparison signal is high-level,
14 otherwise the first comparison signal is low-
15 level;
16 a second phase frequency detector receiving the second
17 reference signal, receiving the oscillation
18 signal, and generating a second detection signal;
19 a second low-pass filter receiving the second detection
20 signal and outputting the dc component of the
21 second detection signal;
22 a second comparator receiving the dc component of the
23 second detection signal and generating a second
24 comparison signal wherein when the second
25 reference frequency lies above the oscillation
26 frequency, the second comparison signal is high-
27 level, otherwise the second comparison signal is
28 low-level; and
29 an exclusive gate receiving the first comparison
30 signal, receiving the second comparison signal,
31 and generating the comparison signal.

1 12. The digital adjustable chip oscillator as claimed
2 in claim 11, wherein the first low-pass filter and the
3 second low-pass filter are both switch capacitance filters.

1 13. The digital adjustable chip oscillator as claimed
2 in claim 1, wherein the voltage control oscillator and the
3 digital tuning circuit both have power save mode.

1 14. A digital adjustable chip oscillator, comprising: ✓
2 a voltage control oscillator generating an oscillation
3 signal, receiving a control voltage to adjust the
4 frequency of the oscillation signal, and receiving
5 an operating voltage to stabilize the frequency of
6 the oscillation signal;
7 a reference voltage circuit generating a reference
8 voltage;
9 a voltage regulation circuit receiving the reference
10 voltage and generating the operating voltage; and
11 a digital tuning circuit receiving a digital code to
12 adjust the control voltage and receiving the
13 operating voltage to stabilize the control
14 voltage.

1 15. The digital adjustable chip oscillator as claimed
2 in claim 14, wherein the voltage control oscillator is a
3 relaxation oscillator.

1 16. The digital adjustable chip oscillator as claimed
2 in claim 14, wherein the reference voltage circuit is a
3 bandgap reference voltage circuit.

1 17. The digital adjustable chip oscillator as claimed
2 in claim 5, further comprising a prescaler receiving the
3 oscillation signal and generating a period dividing signal
4 according to a period dividing code.

1 18. The digital adjustable chip oscillator as claimed
2 in claim 14, wherein the voltage regulation circuit
3 comprises:

4 an operational transconductance amplifier receiving the
5 reference voltage, receiving a loop voltage, and
6 outputting a bias voltage;
7 a transistor receiving the bias voltage, outputting a
8 current, and outputting the operating voltage; and
9 a loop circuit receiving the current and outputting the
10 loop voltage.

1 19. The digital adjustable chip oscillator as claimed
2 in claim 14, wherein the digital tuning circuit comprises:

3 a plurality of current mirrors receiving a bias voltage
4 to generate a plurality of bias currents
5 corresponding to the bit of the digital code and
6 receiving the operating voltage to stabilize the
7 plurality of bias currents;
8 a transistor receiving the plurality of bias currents
9 to generate the control voltage; and
10 a plurality of switches coupled to the plurality of
11 current mirrors and the transistor and receiving
12 the digital code to select the plurality of
13 current mirrors.

1 20. The digital adjustable chip oscillator as claimed
2 in claim 14, wherein the digital tuning circuit further
3 comprises:

4 an operational transconductance amplifier receiving the
5 reference voltage, receiving a loop voltage, and
6 outputting the bias voltage;

7 a transistor receiving the bias voltage, outputting a
8 reference current, and proportioning the bias
9 current of the plurality of current mirrors to the
10 reference current wherein the bias voltage is
11 coupled to the plurality of current mirrors; and

12 a loop circuit receiving the reference current and
13 outputting the loop voltage.

1 21. The digital adjustable chip oscillator as claimed
2 in claim 14, wherein the digital tuning circuit further
3 comprises:

4 a plurality of charge current mirrors receiving a bias
5 voltage to generate a plurality of bias currents
6 corresponding to the bit of the digital code and
7 receiving the operating voltage to stabilize the
8 plurality of bias currents;

9 a plurality of discharge current mirrors receiving the
10 bias current to generate a plurality of bias
11 currents corresponding to the bit of the digital
12 code;

13 a transistor receiving the plurality of bias currents
14 to generate the control voltage;

15 a plurality of first switches coupled to the plurality
16 of current mirrors and the transistor and

17 receiving the digital code to select the plurality
18 of charge current mirrors; and
19 a plurality of second switches coupled to the plurality
20 of current mirrors and the transistor and
21 receiving the digital code to select the plurality
22 of charge current mirrors.

1 22. The digital adjustable chip oscillator as claimed
2 in claim 14, wherein it further comprises:
3 a frequency detector receiving the oscillation signal,
4 a first reference signal with a first frequency,
5 and a second reference signal with a second
6 frequency, wherein when the oscillation frequency
7 lies between the first frequency and the second
8 frequency, the frequency detector will output a
9 high voltage comparison signal, otherwise the
10 frequency detector will output a low voltage
11 comparison signal;
12 a programmable counter receiving a clock signal to
13 trigger the counting and generating the digital
14 code;
15 a programmable controller receiving the high voltage
16 comparison signal to generate an enable signal
17 directing the frequency detector to hold the high
18 voltage comparison signal and directing the
19 programmable counter to stop counting and hold the
20 digital code; and
21 a programmable memory receiving the enable signal to
22 record the digital code.

1 23. The digital adjustable chip oscillator as claimed
2 in claim 22, wherein the programmable memory comprises:
3 a plurality of decoders; and
4 a plurality of poly-silicon fuses.

1 24. The digital adjustable chip oscillator as claimed
2 in claim 22, wherein the programmable memory is a
3 programmable gate writer.

1 25. The digital adjustable chip oscillator as claimed
2 in claim 22, wherein the frequency detector comprises:
3 a first phase frequency detector receiving the first
4 reference signal, receiving the oscillation
5 signal, and generating a first detection signal;
6 a first low-pass filter receiving the first detection
7 signal and outputting the dc component of the
8 first detection signal;
9 a first comparator receiving the dc component of the
10 first detection signal and generating a first
11 comparison signal wherein when the first reference
12 frequency lies above the oscillation frequency,
13 the first comparison signal is high-level,
14 otherwise the first comparison signal is low-
15 level;
16 a second phase frequency detector receiving the second
17 reference signal, receiving the oscillation
18 signal, and generating a second detection signal;
19 a second low-pass filter receiving the second detection
20 signal and outputting the dc component of the
21 second detection signal;

22 a second comparator receiving the dc component of the
23 second detection signal and generating a second
24 comparison signal wherein when the second
25 reference frequency lies above the oscillation
26 frequency, the second comparison signal is high-
27 level, otherwise the second comparison signal is
28 low-level; and
29 an exclusive gate receiving the first comparison
30 signal, receiving the second comparison signal,
31 and generating the comparison signal.

1 26. The digital adjustable chip oscillator as claimed
2 in claim 25, wherein the first low-pass filter and the
3 second low-pass filter are both switch capacitance filters.

1 27. A digital adjustable chip oscillator, comprising:
2 a voltage control oscillator generating an oscillation
3 signal and receiving a control voltage to control
4 the frequency of the oscillation signal;
5 a frequency-to-voltage converter receiving the
6 oscillation signal and generating a loop voltage
7 based on an operating voltage and a first voltage;
8 an active comparison filter receiving the loop voltage,
9 receiving a second voltage, and generating the
10 control voltage; and
11 a first programmable controller receiving a first
12 digital code, receiving the operating voltage, and
13 generating the second voltage.

1 28. The digital adjustable chip oscillator as claimed
2 in claim 27, further comprising a reference voltage circuit

3 generating the reference voltage wherein the reference
4 voltage circuit is a bandgap reference voltage circuit.

1 29. The digital adjustable chip oscillator as claimed
2 in claim 27, further comprising a voltage regulation circuit
3 receiving the reference voltage and generating the operating
4 voltage.

1 30. The digital adjustable chip oscillator as claimed
2 in claim 27, wherein the voltage regulation circuit
3 comprises:

4 an operational transconductance amplifier receiving the
5 reference voltage, receiving a loop voltage, and
6 outputting a bias voltage;
7 a transistor receiving the bias voltage, outputting a
8 current, and outputting the operating voltage; and
9 a loop circuit receiving the current and outputting the
10 loop voltage.

1 31. The digital adjustable chip oscillator as claimed
2 in claim 27, further comprising a prescaler receiving the
3 oscillation signal, generating a period dividing signal
4 based on a period dividing code, and outputting the a period
5 dividing signal to the frequency-to-voltage converter.

1 32. The digital adjustable chip oscillator as claimed
2 in claim 31, further comprising a delay circuit receiving
3 the period dividing signal, generating a delay signal, and
4 outputting the delay signal to the frequency-to-voltage
5 converter wherein the operating period of the delay signal

6 satisfies the requirement of the frequency-to-voltage
7 converter.

1 33. The digital adjustable chip oscillator as claimed
2 in claim 27, wherein the first programmable controller
3 comprises:

4 a resistor serial having a plurality of resistors,
5 receiving the operating voltage, and generating
6 the second voltage from the output end;
7 a plurality of switches coupled to the corresponding
8 connection point of the plurality of resistors and
9 the output end of the programmable controller; and
10 a decoder receiving the first digital code to select
11 the corresponding switch.

1 34. The digital adjustable chip oscillator as claimed
2 in claim 27, wherein the frequency-to-voltage converter
3 comprises:

4 a first capacitor;
5 a second capacitor;
6 an amplifier having an input end, a reversed-phase
7 input end, and an output end wherein the input end
8 of the amplifiers is coupled to the first voltage;
9 a third capacitor coupled to the reversed-phase input
10 end of the amplifier and the output end of the
11 amplifier;
12 a first switch coupled to the input end of the
13 frequency-to-voltage converter and the reversed-
14 phase input end of the reversed-phase amplifier
15 wherein the control end of the first switch

16 receives a signal having the phase opposite to the
17 phase of the oscillation signal;
18 a second switch coupled to the reversed-phase input end
19 of the reversed-phase amplifier and the second
20 capacitor wherein the control end of the second
21 switch receives the output signal of the voltage
22 control oscillator;
23 a voltage control current source coupled to the second
24 capacitor wherein the input end of the voltage
25 control current source receives the output end
26 voltage of the reversed-phase amplifier and the
27 output end of the voltage control current source
28 generates a balance current; and
29 a current-to-voltage converter circuit of which the
30 input end is coupled to the input end of the
31 voltage control current source and the output end
32 is coupled to a resistor wherein the current of
33 the resistor is proportional to the balance
34 current.

1 35. The digital adjustable chip oscillator as claimed
2 in claim 27, wherein the digital adjustable chip oscillator
3 further comprises a second programmable controller receiving
4 a second digital code to select the input current of the
5 resistor in the current-to-voltage converter circuit.

1 36. The digital adjustable chip oscillator as claimed
2 in claim 35, wherein the second programmable controller
3 comprises:
4 a plurality of current mirrors wherein each bias point
5 of the current mirrors is coupled to the input end

6 of the voltage control current source, the current
7 generated by the output end of the voltage control
8 current source is a multiple of the balance
9 current, and the multiplication factor corresponds
10 to the bit of the digital code; and
11 a plurality of switches coupled to the output end of
12 the correspondent above-mentioned plurality of
13 current mirrors and the output end of the
14 frequency-to-voltage converter and receiving the
15 digital code to select the plurality of current
16 mirrors.

1 37. The digital adjustable chip oscillator as claimed
2 in claim 27, wherein the active comparison filter is a
3 proportional integral filter.

1 38. The digital adjustable chip oscillator as claimed
2 in claim 27, wherein the active comparison filter comprises:
3 a differential amplifier having an input end, a
4 reversed-phase input end, and an output end
5 wherein the input end of the differential
6 amplifier receives the second voltage
7 a first resistor of which one end receives the loop
8 voltage and the other end is coupled to the
9 reversed-phase input end of the differential
10 amplifier;
11 a first capacitor coupled to the reversed-phase input
12 end of the differential amplifier and the output
13 end of the differential amplifier;

14 a second resistor of which one end is coupled to the
15 reversed-phase input end of the differential
16 amplifier; and
17 a second capacitor coupled to the other end of the
18 second resistor and the output end of the
19 differential amplifier.

1 39. The digital adjustable chip oscillator as claimed
2 in claim 27, further comprising a voltage limiter receiving
3 the control voltage output by the active comparison filter
4 and limiting the control voltage in the input range of the
5 voltage control oscillator.

1 40. The digital adjustable chip oscillator as claimed
2 in claim 27, wherein the voltage control oscillator
3 comprises a plurality of differential delay units connected
4 in the form of a ring wherein each of the differential delay
5 unit has a control end to receive the control voltage and
6 adjust the delay time, and has a pair of differential inputs
7 and a pair of differential outputs.

1 41. The digital adjustable chip oscillator as claimed
2 in claim 40, wherein the voltage control oscillator further
3 comprises a differential single-end converter having a pair
4 of differential inputs and a single-end output end wherein
5 the pair of differential inputs of the differential single-
6 end converter is coupled to an output pair of the
7 differential delay unit.

1 42. The digital adjustable chip oscillator as claimed
2 in claim 40, wherein the voltage control oscillator further

3 comprises an output buffer of which the input end is coupled
4 to the single-end output end of the differential single-end
5 converter, and the signal of the output end is a full
6 amplitude signal.

1 43. The digital adjustable chip oscillator as claimed
2 in claim 27, further comprising:

3 a frequency detector receiving the oscillation signal,
4 a first reference signal with a first frequency,
5 and a second reference signal with a second
6 frequency, wherein when the oscillation frequency
7 lies between the first frequency and the second
8 frequency, the frequency detector will output a
9 high voltage comparison signal, otherwise the
10 frequency detector will output a low voltage
11 comparison signal;
12 a programmable counter receiving a clock signal to
13 trigger the counting and generating the first
14 digital code;
15 a programmable controller receiving the high voltage
16 comparison signal to generate an enable signal
17 directing the frequency detector to hold the high
18 voltage comparison signal and directing the
19 programmable counter to stop counting and hold the
20 digital code; and
21 a programmable memory receiving the enable signal to
22 record the digital code.

1 44. The digital adjustable chip oscillator as claimed
2 in claim 43, wherein the programmable memory is a
3 programmable fuse.

1 45. The digital adjustable chip oscillator as claimed
2 in claim 1, wherein the programmable memory is a
3 programmable gate writer.

1 46. The digital adjustable chip oscillator as claimed
2 in claim 27, further comprising:

3 a frequency detector receiving the oscillation signal,
4 a first reference signal with a first frequency,
5 and a second reference signal with a second
6 frequency, wherein when the oscillation frequency
7 lies between the first frequency and the second
8 frequency, the frequency detector will output a
9 high voltage comparison signal, otherwise the
10 frequency detector will output a low voltage
11 comparison signal;

12 a programmable counter receiving a clock signal to
13 trigger the counting and generating the first
14 digital code and the second digital code;

15 a programmable controller receiving the high voltage
16 comparison signal to generate an enable signal
17 directing the frequency detector to hold the high
18 voltage comparison signal and directing the
19 programmable counter to stop counting and hold the
20 first digital code and the second digital code;
21 and

22 a programmable memory receiving the enable signal to
23 record the first digital code and the second
24 digital code.

1 47. The digital adjustable chip oscillator as claimed
2 in claim 43, wherein the frequency detector comprises:
3 a first phase frequency detector receiving the first
4 reference signal, receiving the oscillation
5 signal, and generating a first detection signal;
6 a first low-pass filter receiving the first detection
7 signal and outputting the dc component of the
8 first detection signal;
9 a first comparator receiving the dc component of the
10 first detection signal and generating a first
11 comparison signal wherein when the first reference
12 frequency lies above the oscillation frequency,
13 the first comparison signal is high-level,
14 otherwise the first comparison signal is low-
15 level;
16 a second phase frequency detector receiving the second
17 reference signal, receiving the oscillation
18 signal, and generating a second detection signal;
19 a second low-pass filter receiving the second detection
20 signal and outputting the dc component of the
21 second detection signal;
22 a second comparator receiving the dc component of the
23 second detection signal and generating a second
24 comparison signal wherein when the second
25 reference frequency lies above the oscillation
26 frequency, the second comparison signal is high-
27 level, otherwise the second comparison signal is
28 low-level; and

29 an exclusive gate receiving the first comparison
30 signal, receiving the second comparison signal,
31 and generating the comparison signal.

1 48. The digital adjustable chip oscillator as claimed
2 in claim 47, wherein the first low-pass filter and the
3 second low-pass filter are both switch capacitance filters.

1 49. A digital adjustable chip oscillator, comprising:
2 a voltage control oscillator generating an oscillation
3 signal and receiving a control voltage to control
4 the frequency of the oscillation signal;
5 a frequency-to-voltage converter receiving the
6 oscillation signal and generating a loop voltage
7 based on an operating voltage and a first voltage;
8 an active comparison filter receiving the loop voltage,
9 receiving a second voltage, and generating the
10 control voltage; and
11 a first programmable controller receiving a first
12 digital code, receiving the operating voltage, and
13 generating the second voltage.
14 a frequency detector receiving the oscillation signal,
15 a first reference signal with a first frequency,
16 and a second reference signal with a second
17 frequency, wherein when the frequency of the
18 oscillation signal lies between the first
19 frequency and the second frequency, the frequency
20 detector will output a high voltage comparison
21 signal, otherwise the frequency detector will
22 output a low voltage comparison signal;

23 a programmable counter receiving a clock signal to
24 trigger the counting and generating the first
25 digital code;
26 a programmable controller receiving the high voltage
27 comparison signal to generate an enable signal
28 directing the frequency detector to hold the high
29 voltage comparison signal and directing the
30 programmable counter to stop counting and hold the
31 first digital code; and
32 a programmable memory receiving the enable signal to
33 record the first digital code.

1 50. The digital adjustable chip oscillator as claimed
2 in claim 49, further comprising a reference voltage circuit
3 generating the reference voltage wherein the reference
4 voltage circuit is a bandgap reference voltage circuit.

1 51. The digital adjustable chip oscillator as claimed
2 in claim 49, further comprising a voltage regulation circuit
3 receiving the reference voltage and generating the operating
4 voltage.

1 52. The digital adjustable chip oscillator as claimed
2 in claim 49, wherein the voltage regulation circuit
3 comprises:

4 an operational transconductance amplifier receiving the
5 reference voltage, receiving a loop voltage, and
6 outputting a bias voltage;
7 a transistor receiving the bias voltage, outputting a
8 current, and outputting the operating voltage; and

9 a loop circuit receiving the current and outputting the
10 loop voltage.

1 53. The digital adjustable chip oscillator as claimed
2 in claim 49, wherein the first programmable controller
3 comprises:

4 a resistor serial having a plurality of resistors,
5 receiving the operating voltage, and generating
6 the second voltage from the output end;
7 a plurality of switches coupled to the corresponding
8 connection point of the plurality of resistors and
9 the output end of the programmable controller; and
10 a decoder receiving the first digital code to select
11 the corresponding switch.

1 54. The digital adjustable chip oscillator as claimed
2 in claim 49, wherein the frequency-to-voltage converter
3 comprises:

4 a first capacitor;
5 a second capacitor;
6 an amplifier having an input end, a reversed-phase
7 input end, and an output end wherein the input end
8 of the amplifiers is coupled to the first voltage;
9 a third capacitor coupled to the reversed-phase input
10 end of the amplifier and the output end of the
11 amplifier;
12 a first switch coupled to the input end of the
13 frequency-to-voltage converter and the reversed-
14 phase input end of the reversed-phase amplifier
15 wherein the control end of the first switch

16 receives a signal having a phase opposite to the
17 phase of the oscillation signal;
18 a second switch coupled to the reversed-phase input end
19 of the reversed-phase amplifier and the second
20 capacitor wherein the control end of the second
21 switch receives the output signal of the voltage
22 control oscillator;
23 a voltage control current source coupled to the second
24 capacitor wherein the input end of the voltage
25 control current source receives the output end
26 voltage of the reversed-phase amplifier and the
27 output end of the voltage control current source
28 generates a balance current; and
29 a current-to-voltage converter circuit of which the
30 input end is coupled to the input end of the
31 voltage control current source and the output end
32 is coupled to a resistor wherein the current of
33 the resistor is proportional to the balance
34 current.

1 55. The digital adjustable chip oscillator as claimed
2 in claim 49, further comprising a prescaler receiving the
3 oscillation signal, generating a period dividing signal
4 based on a period dividing code, and outputting the period
5 dividing signal to the frequency-to-voltage converter.

1 56. The digital adjustable chip oscillator as claimed
2 in claim 55, further comprising a delay circuit receiving
3 the period dividing signal, generating a delay signal, and
4 outputting the delay signal to the frequency-to-voltage
5 converter wherein the operating period of the delay signal

6 satisfies the requirement of the frequency-to-voltage
7 converter.

1 57. The digital adjustable chip oscillator as claimed
2 in claim 49, further comprising a second programmable
3 controller receiving a second digital code to select the
4 input current of the resistor in the current-to-voltage
5 converter circuit.

1 58. The digital adjustable chip oscillator as claimed
2 in claim 57, wherein the second programmable controller
3 comprises:

4 a plurality of current mirrors wherein each bias point
5 of the current mirrors is coupled to the input end
6 of the voltage control current source, the current
7 generated by the output end of the voltage control
8 current source is a multiple of the balance
9 current, and the multiplication factor corresponds
10 to the bit of the digital code; and

11 a plurality of switches coupled to the output end of
12 the correspondent above-mentioned plurality of
13 current mirrors and the output end of the
14 frequency-to-voltage converter and receiving the
15 digital code to select the plurality of current
16 mirrors.

1 59. The digital adjustable chip oscillator as claimed
2 in claim 49, wherein the active comparison filter is a
3 proportional integral filter.

1 60. The digital adjustable chip oscillator as claimed
2 in claim 49, wherein the active comparison filter comprises:

3 a differential amplifier having an input end, a
4 reversed-phase input end, and an output end
5 wherein the input end of the differential
6 amplifier receives the second voltage

7 a first resistor of which one end receives the loop
8 voltage and the other end is coupled to the
9 reversed-phase input end of the differential
10 amplifier;

11 a first capacitor coupled to the reversed-phase input
12 end of the differential amplifier and the output
13 end of the differential amplifier;

14 a second resistor of which one end is coupled to the
15 reversed-phase input end of the differential
16 amplifier; and

17 a second capacitor coupled to the other end of the
18 second resistor and the output end of the
19 differential amplifier.

1 61. The digital adjustable chip oscillator as claimed
2 in claim 49, further comprising a voltage limiter receiving
3 the control voltage output by the active comparison filter
4 and limiting the control voltage in the input range of the
5 voltage control oscillator.

1 62. The digital adjustable chip oscillator as claimed
2 in claim 49, wherein the voltage control oscillator
3 comprises a plurality of differential delay units connected
4 in the form of a ring wherein each of the differential delay

5 unit has a control end to receive the control voltage and
6 adjust the delay time, and has a pair of differential inputs
7 and a pair of differential outputs.

1 63. The digital adjustable chip oscillator as claimed
2 in claim 62, wherein the voltage control oscillator further
3 comprises a differential single-end converter having a pair
4 of differential inputs and a single-end output end wherein
5 the pair of differential inputs of the differential single-
6 end converter is coupled to an output pair of the
7 differential delay unit.

1 64. The digital adjustable chip oscillator as claimed
2 in claim 63, wherein the voltage control oscillator further
3 comprises an output buffer of which the input end is coupled
4 to the single-end output end of the differential single-end
5 converter, and the signal of the output end is a full
6 amplitude signal.

1 65. The digital adjustable chip oscillator as claimed
2 in claim 49, wherein the programmable memory is a
3 programmable fuse.

1 66. The digital adjustable chip oscillator as claimed
2 in claim 49, wherein the programmable memory is a
3 programmable gate writer.

1 67. The digital adjustable chip oscillator as claimed
2 in claim 49, wherein the frequency detector comprises:
3 a first phase frequency detector receiving the first
4 reference signal, receiving the oscillation
5 signal, and generating a first detection signal;

6 a first low-pass filter receiving the first detection
7 signal and outputting the dc component of the
8 first detection signal;
9 a first comparator receiving the dc component of the
10 first detection signal and generating a first
11 comparison signal wherein when the first reference
12 frequency lies above the oscillation frequency,
13 the first comparison signal is high-level,
14 otherwise the first comparison signal is low-
15 level;
16 a second phase frequency detector receiving the second
17 reference signal, receiving the oscillation
18 signal, and generating a second detection signal;
19 a second low-pass filter receiving the second detection
20 signal and outputting the dc component of the
21 second detection signal;
22 a second comparator receiving the dc component of the
23 second detection signal and generating a second
24 comparison signal wherein when the second
25 reference frequency lies above the oscillation
26 frequency, the second comparison signal is high-
27 level, otherwise the second comparison signal is
28 low-level; and
29 an exclusive gate receiving the first comparison
30 signal, receiving the second comparison signal,
31 and generating the comparison signal.

1 68. The digital adjustable chip oscillator as claimed
2 in claim 67, wherein the first low-pass filter and the
3 second low-pass filter are both switch capacitance filters.